

EXHIBIT Y

Exhibit A (Supplemental)

U.S. Pat. No. 9,218,156
Claim 7

'156 PATENT**7. A **device** comprising:**

at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,

wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least $X=5\%$ of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least $X\%$ of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least $Y=0.05\%$ from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

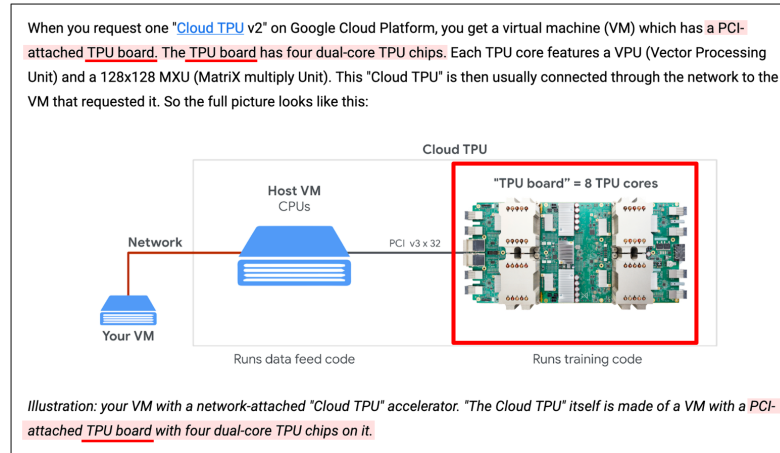
at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

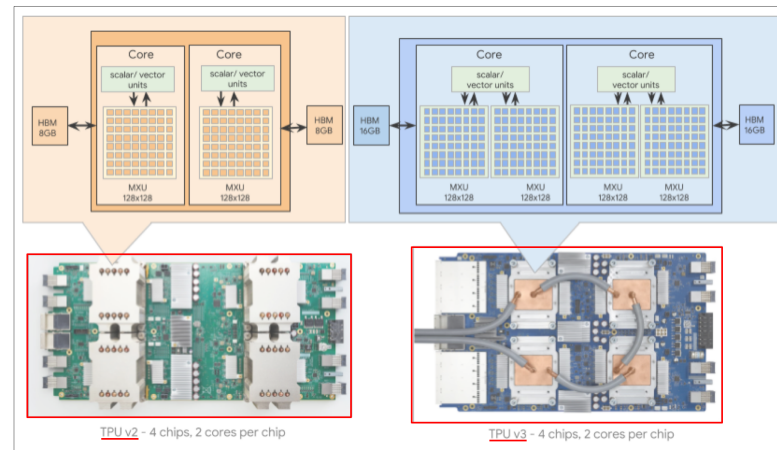
wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

SUPPLEMENTAL INFRINGEMENT EVIDENCE

As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed "device.":



<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2>¹



<https://cloud.google.com/tpu/docs/system-architecture>

¹ Unless indicated otherwise, color-coded annotations have been added in order to identify relevant components and features of the Accused Products.

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SUPPLEMENTAL INFRINGEMENT EVIDENCE

As demonstrated below, the Accused Products include multiple components that, separately and independently, meet all the requirements of the claimed "device." For example, a "TPU Chip" satisfies these requirements:

When you request one "Cloud TPU v2" on Google Cloud Platform, you get a virtual machine (VM) which has a PCI-attached TPU board. The TPU board has four dual-core TPU chips. Each TPU core features a VPU (Vector Processing Unit) and a 128x128 MXU (Matrix multiply Unit). This "Cloud TPU" is then usually connected through the network to the VM that requested it. So the full picture looks like this:

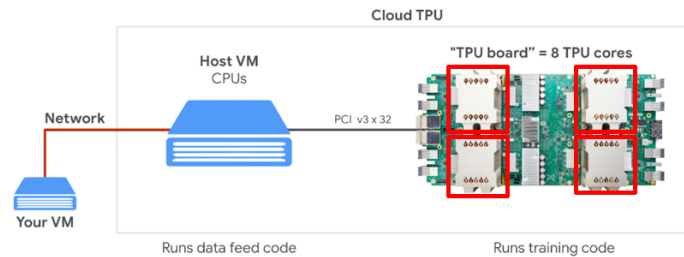
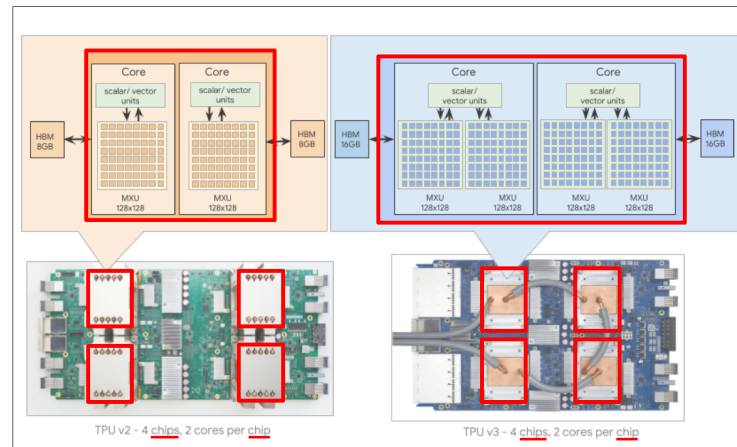


Illustration: your VM with a network-attached "Cloud TPU" accelerator. "The Cloud TPU" itself is made of a VM with a PCI-attached TPU board with four dual-core TPU chips on it.

<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2>



<https://cloud.google.com/tpu/docs/system-architecture>

See also generally Norrie et al., "Google's Training Chips Revealed: TPuv2 and TPuv3" (Presented at HotChips Conference, Aug. 2020)

² Unless indicated otherwise, color-coded annotations have been added to the figures in this chart to highlight relevant teachings of the prior art.

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wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

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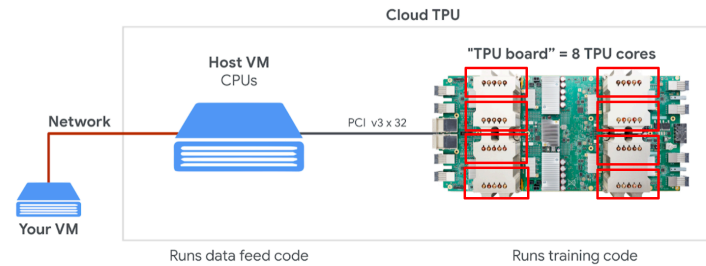
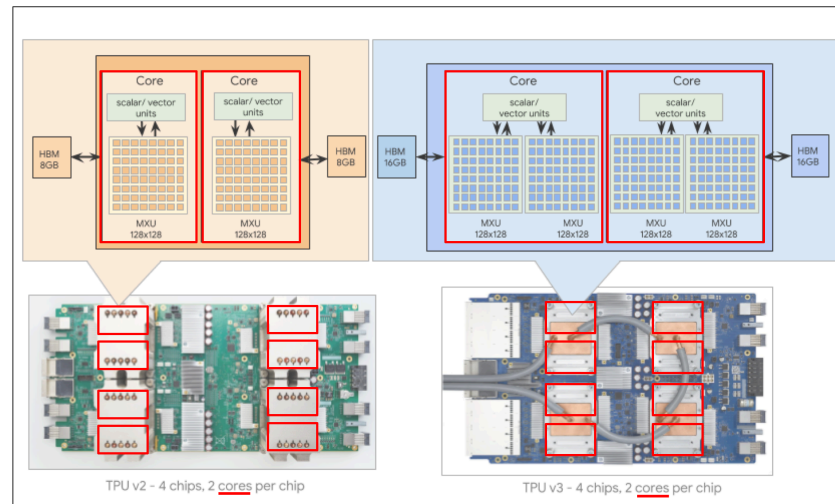


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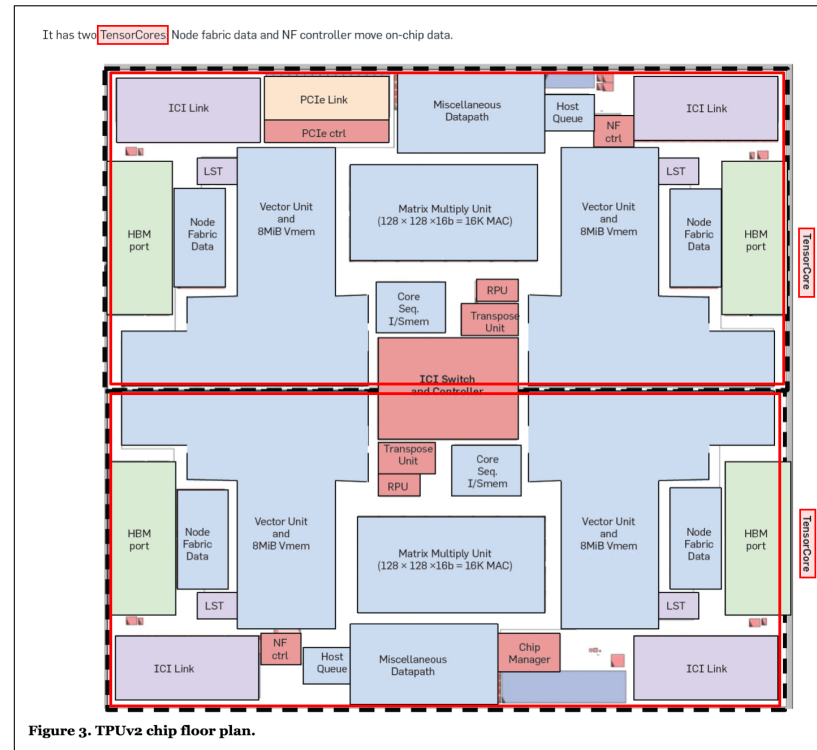
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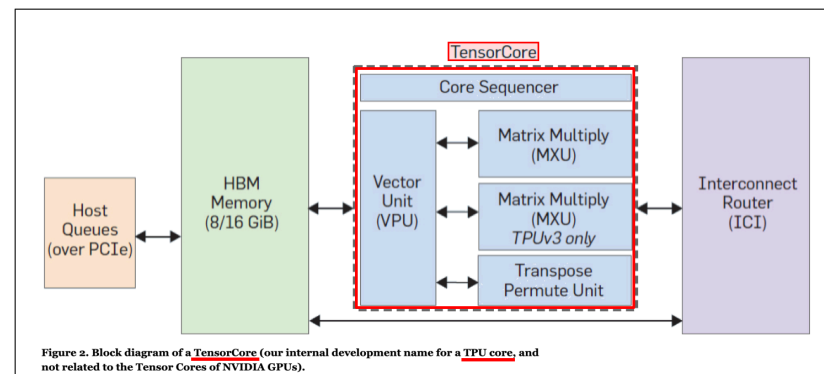
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wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

SUPPLEMENTAL INFRINGEMENT EVIDENCE

<https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks>



Id.

See also GOOG-SING-SC-000001-454.

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SUPPLEMENTAL INFRINGEMENT EVIDENCE

TPU v2 - 4 chips, 2 cores per chip

TPU v3 - 4 chips, 2 cores per chip

Each TPU core has scalar, vector, and matrix units (MXU). The MXU provides the bulk of the compute power in a TPU chip. Each MXU is capable of performing 16K multiply-accumulate operations in each cycle. While the MXU inputs and outputs are 32-bit floating point values, the MXU performs multiplies at reduced bfloat16 precision. Bfloat16 is a 16-bit floating point representation that provides better training and model accuracy than the IEEE half-precision representation.

<https://cloud.google.com/tpu/docs/system-architecture>

	sign	exponent	fraction
bfloat16 range: $\sim 1e^{-38}$ to $\sim 3e^{38}$	1 bit	8 bits	7 bits
float32 range: $\sim 1e^{-38}$ to $\sim 3e^{38}$	1 bit	8 bits	23 bits
float16 range: $\sim 5.9e^{-8}$ to $6.5e^4$	1 bit	5 bits	10 bits

<https://cloud.google.com/tpu/docs/bfloat16>

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SUPPLEMENTAL INFRINGEMENT EVIDENCE

Systolic array

The MXU implements matrix multiplications in hardware using a so-called "systolic array" architecture in which data elements flow through an array of hardware computation units. (In medicine, "systolic" refers to heart contractions and blood flow, here to the flow of data.)

The basic element of a matrix multiplication is a dot product between a line from one matrix and a column from the other matrix (see illustration at the top of this section). For a matrix multiplication $Y=X*W$, one element of the result would be:

$$Y[2,0] = X[2,0]*W[0,0] + X[2,1]*W[1,0] + X[2,2]*W[2,0] + \dots + X[2,n]*W[n,0]$$

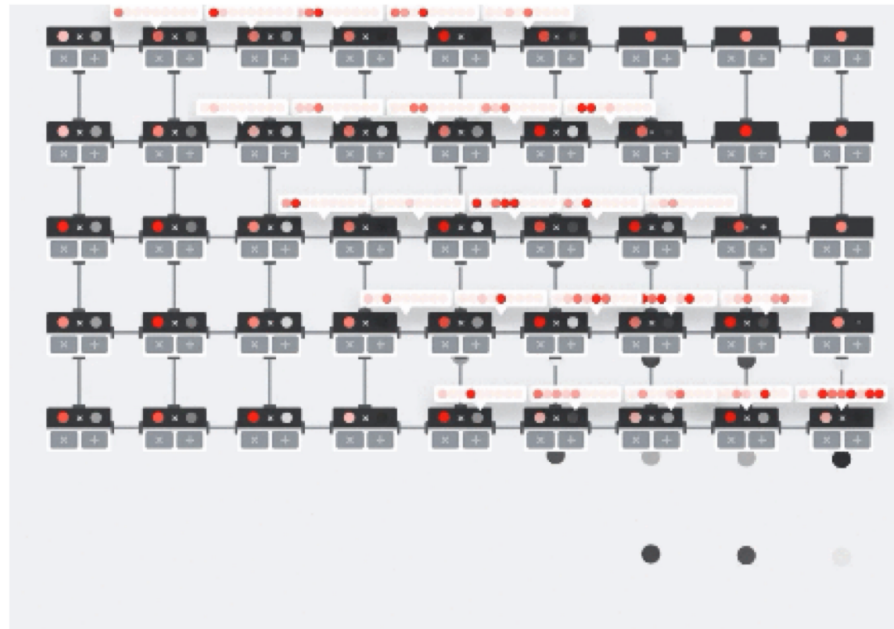
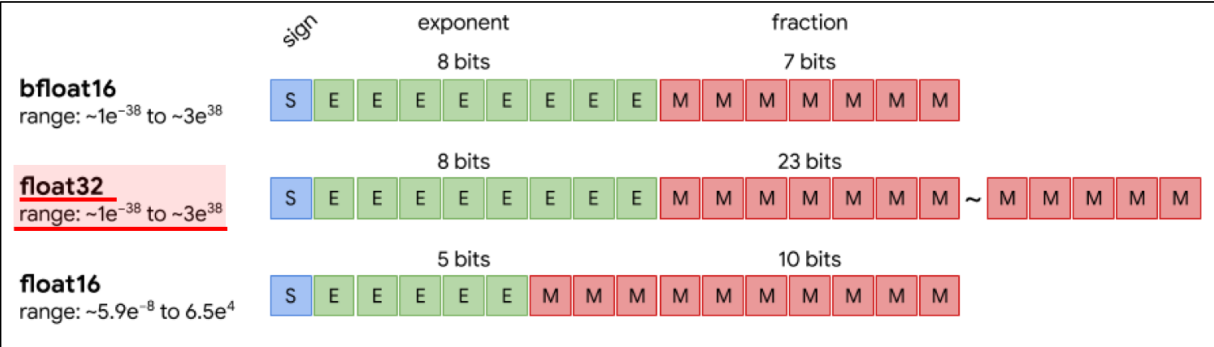


Illustration: the MXU systolic array. The compute elements are multiply-accumulators. The values of one matrix are loaded into the array (red dots). Values of the other matrix flow through the array (grey dots). Vertical lines propagate the values up. Horizontal lines propagate partial sums. It is left as an exercise to the user to verify that as the data flows through the array, you get the result of the matrix multiplication coming out of the right side.

<https://codelabs.developers.google.com/codelabs/keras-flowers-convnets/#2>

See also GOOG-SING-SC-000001-10, 13-30, 33-61, 228-292, 315-373, 396-444, 449-454.

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<p>7. A device comprising: at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value, wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit</p> <p>wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p>	<ul style="list-style-type: none"> “Each TPU core has scalar, vector, and matrix units (MXU). The MXU provides the bulk of the compute power in a TPU chip. Each MXU is capable of performing 16K multiply-accumulate operations in each cycle. While the MXU inputs and outputs are 32-bit floating point values, the MXU performs multiplies at reduced bfloat16 precision. Bfloat16 is a 16-bit floating point representation that provides better training and model accuracy than the IEEE half-precision representation.” https://cloud.google.com/tpu/docs/system-architecture “The following figure shows three floating-point[] formats <ul style="list-style-type: none"> fp32 - IEEE single-precision floating-point fp16 - IEEE half-precision floating point bfloat16 - 16-bit <i>brain floating point</i>” https://cloud.google.com/tpu/docs/bfloat16 <div data-bbox="772 526 1917 850"> <p>The diagram illustrates the bit layouts for three floating-point formats:</p> <ul style="list-style-type: none"> bfloat16: range: $\sim 1e^{-38}$ to $\sim 3e^{38}$. It consists of 1 sign bit (S), 8 exponent bits (E), and 7 fraction bits (M). float32: range: $\sim 1e^{-38}$ to $\sim 3e^{38}$. It consists of 1 sign bit (S), 8 exponent bits (E), and 23 fraction bits (M). float16: range: $\sim 5.9e^{-8}$ to $6.5e^4$. It consists of 1 sign bit (S), 5 exponent bits (E), and 10 fraction bits (M). </div> <p><i>Id.</i></p> <p>See also GOOG-SING-SC-45-61, 435-444, 449-454.</p>

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7. A device comprising:

at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,

wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least $X=5\%$ of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least $X\%$ of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least $Y=0.05\%$ from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;

at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;

wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine; and,

wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.

SUPPLEMENTAL INFRINGEMENT EVIDENCE

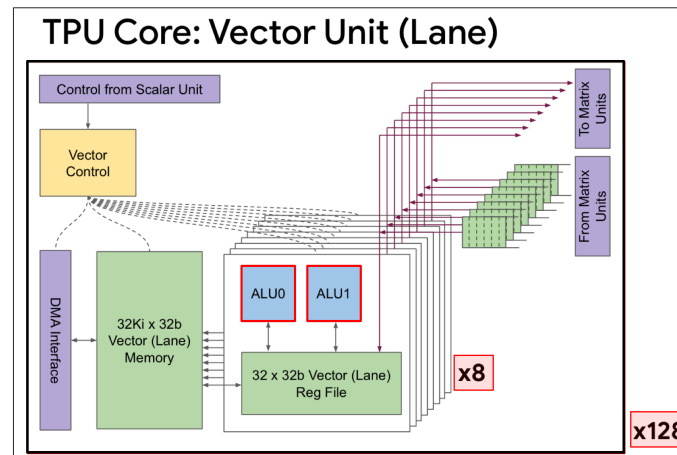
The Accused Products independently meet this claim limitation for each "device" identified above:

We cannot reveal technology details of our chip partner. Although it is in a larger, older technology, the TPUv2 die size is less than 3/4s of the GPU. TPUv3 is 6% larger in that same technology. TDP stands for Thermal Design Power. The Volta has 80 symmetric multiprocessors.

Feature	TPUv1	TPUv2	TPUv3	Volta
Peak TeraFLOPS/Chip	92 (8b int)	46 (16b) 3 (32b)	123 (16b) 4 (32b)	125 (16b) 16 (32b)
Network links x Gbits/s/Chip	--	4 x 496	4 x 656	6 x 200
Max chips/supercomputer	--	256	1024	Varies
Peak PetaFLOPS/supercomputer	--	11.8	126	Varies
Bisection Terabits/supercomputer	--	15.9	42.0	Varies
Clock Rate (MHz)	700	700	940	1530
TDP (Watts)/Chip	75	280	450	450
TDP (Kwatts)/supercomputer	--	124	594	Varies
Die Size (mm ²)	<331	<611	<648	815
Chip Technology	28nm	>12nm	>12nm	12nm
Memory size (on/off-chip)	28MiB/8GiB	32MiB/16GiB	32MiB/32GiB	36MiB/32GiB
Memory GB/s/Chip	34	700	900	900
MXUs/Core	1	1	2	8
MXU Size	256x256	128x128	128x128	4x4
Cores/Chip	1	2	2	80
Chips/CPU Host	4	4	8	8 or 16

Table 3. Key processor features.

<https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext>



Norrie et al., "Google's Training Chips Revealed: TPUv2 and TPUv3" (Presented at HotChips Conference, Aug. 2020)

See also GOOG-SING-SC-000001-454.